

# WEST Search History

DATE: Wednesday, December 19, 2007

<u>Hide?</u>	<u>Set Name</u>	<u>Query</u>	<u>Hit Count</u>
<i>DB=PGPB,USPT,USOC; PLUR=YES; OP=ADJ</i>			
<input type="checkbox"/>	L19	L18 and range.clm.	1
<input type="checkbox"/>	L18	L17 and contiguous.clm.	7
<input type="checkbox"/>	L17	(monitor\$ near execution).clm.	612
<input type="checkbox"/>	L16	L15 and (monitor\$ same performance)	65
<input type="checkbox"/>	L15	L14 and instruction cache	246
<input type="checkbox"/>	L14	L12 and (counting or counter or count or counted)	502
<i>DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=ADJ</i>			
<input type="checkbox"/>	L13	L12	3
<i>DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=ADJ</i>			
<input type="checkbox"/>	L12	L11 and performance	684
<input type="checkbox"/>	L11	L7 and (instruction near2 range)	985
<input type="checkbox"/>	L10	L9 and counting	34
<input type="checkbox"/>	L9	L8 and monitor\$	134
<input type="checkbox"/>	L8	L7 and (contiguous range)	212
<input type="checkbox"/>	L7	identif\$ same instruction	119582
<input type="checkbox"/>	L6	L5 and (contiguous range)	1
<input type="checkbox"/>	L5	L4 and (instruction near2 range)	37
<input type="checkbox"/>	L4	L3 and monitor\$ and count\$	887
<input type="checkbox"/>	L3	(717/124  717/125  717/126  717/127  717/128  717/129  717/130  717/131  717/132  717/133  717/134  717/135).ccls.	3507
<input type="checkbox"/>	L2	L1 and (contiguous range).clm.	18
<input type="checkbox"/>	L1	(identif\$ same instruction).clm.	38183

END OF SEARCH HISTORY

**Web**Results 1 - 10 of about 877 for "**range of instruction**" counting contiguous. (0.09 seconds)**Network processors: a perspective on market requirements ...**

restricted **range of instruction**-set permutations. Close to ... non-contiguous registers holding long operands, and. other application-specific needs. ...  
[ieeexplore.ieee.org/iel5/7307/19761/00915058.pdf?arnumber=915058](http://ieeexplore.ieee.org/iel5/7307/19761/00915058.pdf?arnumber=915058) - [Similar pages](#)

**Techniques for accurate performance evaluation in architecture ...**

also designed to cover as wide a **range of instruction** set architectures as possible and,  
... instruction word into a set of contiguous nonoverlapping ...  
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**Network Processors: A Perspective on Market Requirements ...**

restricted **range of instruction**-set permutations. Close to. 500 compiler configurations were ... non-contiguous registers holding long operands, and ...  
[portal.acm.org/ft\\_gateway.cfm?id=367302&type=pdf&dl=GUIDE&id=ACM](http://portal.acm.org/ft_gateway.cfm?id=367302&type=pdf&dl=GUIDE&id=ACM) - [Similar pages](#)

**Methods for increasing instruction-level parallelism in ...**

... in a broad **range of instruction** set architectures including CISC, RISC, ..... **counting** from cycle 0 for the first instruction tuple of the code block. ...  
[www.freepatentsonline.com/6988183.html](http://www.freepatentsonline.com/6988183.html) - 153k - [Cached](#) - [Similar pages](#)

**Simulation of Computer Architectures: Simulators, Benchmarks ...**

Simics supports a wide **range of instruction** sets, including Alpha, PowerPC, ..... Z million contiguous instructions only from somewhere in the benchmark. ...  
[doi.ieeecomputersociety.org/10.1109/TC.2006.44](http://doi.ieeecomputersociety.org/10.1109/TC.2006.44) - [Similar pages](#)

**RISC Processors**

The side effect of providing a wide **range of instruction** ..... struction we can load 128 contiguous bytes from memory into all 32 general-purpose ...  
[www.springerlink.com/index/mkq7398p22351101.pdf](http://www.springerlink.com/index/mkq7398p22351101.pdf) - [Similar pages](#)

**frt(1) UXP/V Fortran frt(1) NAME frt - Fortran Compiler SYNOPSIS ...**

-P n Specifies the **range of instruction** scheduling. ... object program that dynamically checks loop iteration count or array reference dependency, ...  
[hikwww2.fzk.de/hik/orga/horas/hlr/vpp/VPP5000\\_frt.txt](http://hikwww2.fzk.de/hik/orga/horas/hlr/vpp/VPP5000_frt.txt) - 55k - [Cached](#) - [Similar pages](#)

**[PDF] Versatility and VersaBench: A New Metric and a Benchmark Suite for ...**

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have a **range of instruction** mixtures with respect to the integer versus .... from the application as it executes, and partition the trace into contiguous ...  
[cag.csail.mit.edu/versabench/MIT-LCS-TM-646.pdf](http://cag.csail.mit.edu/versabench/MIT-LCS-TM-646.pdf) - [Similar pages](#)

**Instruction-programmable processor with instruction loop cache ...**

3, covering the number of contiguous cache lines including prologue 66p, ..... as inner loop 68 instructions, m being the loop count of inner loop 68). ...  
[www.patentstorm.us/patents/6963965-description.html](http://www.patentstorm.us/patents/6963965-description.html) - 84k - [Cached](#) - [Similar pages](#)

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traces provide a **range of instruction** fetch benefits. Finally, prior .... blocks contiguous in memory. To avoid the overhead of switching ...  
[www.eecs.harvard.edu/alarms/papers/micro2005-hiniker.pdf](http://www.eecs.harvard.edu/alarms/papers/micro2005-hiniker.pdf) - [Similar pages](#)

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